

### REMARKS

Reconsideration of this application as amended is respectfully requested.

Claims 1, 4, 6, 12, 15, 16, 22, 23, and 39 stand rejected under 35 U.S.C. §102(e) as being anticipated by U.S. Patent No. 5,625,845 of Allran (Allran). Claims 2, 3, 5, 13-14, 36-38 stand rejected under 35 U.S.C. §103(a) as being obvious under Allran in view of U.S. Patent No. 6,104,721 of Hsu (Hsu). Claims 7-11, 17-21, 25-34 and 40-44 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Claims 1-23 and 25-34 are unchanged.

The Examiner has rejected claims 1, 4, 6, 12, 15, 16, 22, 23, and 39 under 35 U.S.C. §102(e) as being unpatentable over Allran. The Examiner has stated that

Regarding claims 1, 4, 6, 12, 15, and 16, the claimed digital signal processing (DSP) resource manager reads on DSP resource manager (block 455. Fig. 22

(p. 2 Office Action 07/31/01).

Applicants respectfully submit, however that claims 1, 4, 6, 12, 15, and 16 are not anticipated under 35 U.S.C. §102(e) by Allran. Claims 1, 4, 6, 12, 15, and 16 include the limitations

a digital signal processing (DSP) resource manager configured to ensure DSP availability for each of a number of channels as individual ones of said channels are activated or deactivated.

(Claim 1) (emphasis added).

managing a digital signal processing (DSP) system to ensure DSP availability for each of a number of channels as individual ones of said channels are activated or deactivated.

(Claim 12) (emphasis added).

In contrast, Allran does not disclose configuring to ensure DSP availability for each of a number of channels as individual ones of said channels are activated or deactivated. Allran discloses that

Returning now to FIGS. 31 and 22, resource manager 455 is consulted to determine if loading of the task or module is possible, in view of the current resource allocation and availability in terms of hardware availability, instruction memory availability, data memory availability, cycles per second availability, bus bandwidth availability, direct memory access availability, and interrupt vector availability. If a particular modular multimedia software task is called by the multimedia application software for loading to the digital signal processor, it must not exceed the available resources or the digital signal processor. For example, if the multimedia end devices which are operated by a particular modular multimedia software task are available, and sufficient instruction and data memory space is available, but insufficient digital signal processing cycles per second are not available, the task will not be loaded to the digital signal processor. For an alternative example, if a particular modular multimedia software task is requested to be loaded to the digital signal processor, but all sixteen interrupt vectors are currently being used by other modular multimedia software tasks which are being executed by the digital signal processor, the loading operation is not allowed. If loading is determined to be allowed, the task or module is sent to dsp link editor 453 for "fix-up" operation which at module fixup block 553, task fixup block 555 and segment fixup block 557 to allow writing to the data and instruction memory by blocks 559, 561.

(Allran Col. 25, lines 39-65) (emphasis added).

In other words, Allran uses the DSP resource manager to determine if enough processor resources exist to perform a variety of tasks, rejecting requests to perform a task if the resources are not available. The resources are managed on a per task basis, with no reference made to ensuring processor availability for each of a number of channels. In contrast, Claims 1 and 12 refer to ensuring DSP

availability for each of a number of channels. Given that claims 2-11 depend from claim 1 and claims 13-21 depend from claim 12, applicants submit that claims 4, 6, 15, and 16 are not anticipated under 35 U.S.C. §102 by the reference cited by the Examiner, for at least these reasons.

The Examiner has further stated that

Regarding claims 22, 23, 39, the claimed DSP plurality of digital signal processor (DSP) resources reads on N digital signal processors (column 26, lines 13-19). The claimed resource manager reads on DSP resource manager.

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Applicant assumes that claim 35 is included with these claims as claim 39 is dependent on claim 35. Applicants respectfully submit, however that claims 22, 23, 35, and 39 are not anticipated under 35 U.S.C. §102(e) by Allran. Claims 22, 23, 35, and 39 include the limitations

a DSP resource manager configured to allocate the DSP resources among DSP resource groups according to requirements of a plurality of channels utilizing the DSP resources, allocating sufficient DSP resources to one of the DSP resource groups to process all of the plurality of channels.

(Claim 22) (emphasis added).

An apparatus comprising a means for managing a digital signal processing (DSP) system to ensure DSP availability for each of a number of channels as individual ones of said channels are activated or deactivated.

(Claim 35) (emphasis added).

Applicant would submit that Allran fails to disclose the limitations of claims 22 and 35 for the same reasons given for claims 1 and 12 above. Given that claims 23 and 25-34 depend from claim 22 and claims 36-44 depend from claim 35, applicants submit that claims 23 and 39 are not anticipated under 35 U.S.C. §102 by the reference cited by the Examiner, for at least these reasons.

The Examiner has rejected claims 2, 3, 5, 13-14, and 36-38 under 35 U.S.C. §103 as being unpatentable over Allran in view of Hsu. The Examiner has stated that

Regarding claims 2, 13, 36, Allran teaches digital signal processing system (see the abstract). Allran does not teach a carrier system. However, the use of a carrier system is well known in the art. The claimed carrier system reads on the line card is adapted to receive a plurality of T1 lines, each including 24 channels which may operate at 64 Kbps (column 5, lines 31-33). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to combine Allran's DSP system with Hsu' DSP including carrier system with the motivation being to provide voice digitations in order for proper transmission of signals through the channels.

Regarding claims 3 and 14, 37, 38, the combination of Allran and Hsu discloses a system wherein the carrier system is comprises of T1 lines (column 5, lines 31-33 of Hsu).

Regarding claim 5, the combination of Allran and Hsu teaches a system wherein the channels comprise voice channels (column 5, lines 43-44 of Hsu).

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Claims 2, 3, 5, 13-14, and 36-38 include all limitations disclosed in independent claims 1, 12, and 35 including ensuring DSP availability for each of a number of channels as individual ones of said channels are activated or deactivated. It is submitted Allran does not teach or suggest a combination with Hsu, nor does Hsu teach or suggest a combination with Allran. It is further submitted that combining Allran with Hsu is impermissible hindsight based on applicant's own disclosure. Even if Allran and Hsu were combined, the combination would still lack the element of ensuring DSP availability for each of a number of channels as individual ones of said channels are activated or deactivated. Therefore, claims 2, 3, 5, and 13-14 are not obvious under 35 U.S.C. §103 by the references cited by the Examiner, for at least these reasons.

Applicants therefore submit that the rejections and objections have been overcome. If the Examiner believes a telephone conference would expedite or assist in the allowance of the present application, the Examiner is invited to call Stephen Neal at (408) 720-8300.

If any fee is due not covered by any check submitted please charge  
Deposit Account No. 02-2666.

Respectfully submitted,

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